

Memory Signal Integrity Report

- ❖ Foxconn_SK telecom
- ❖ T99X171T00
- ❖ H5AN4G6NBJR-VKC

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System History

Release Date	Contents	Remarks
2020-03-11	H5AN8G6NCJR-VKC	U503
2020-03-18	H5AN4G6NBJR-VKC	U505

Information & Test Condition

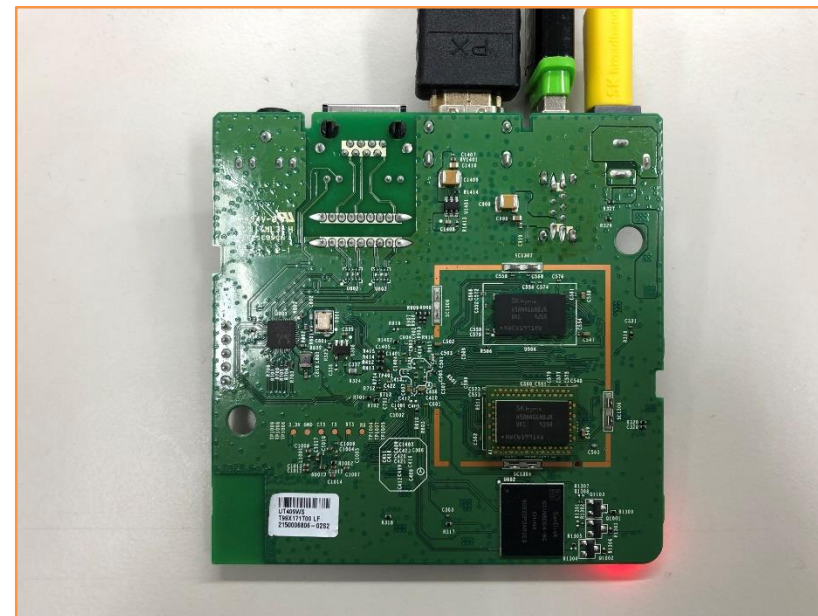
■ System & Memory Information

Model Name	T99X171T00
Application type	OTT Box
PCB Number and Revision	Rev.0
Chipset	Amlogic S905X2
BIOS Version & Date	-
DRAM Part Number	H5AN4G6NBJR-VKC
DRAM Operating Frequency	1333MHz (DDR4-2666)
DRAM Density	4Gb
DRAM pieces	2 ea
DRAM Width	x16

■ Equipment & Test Condition

Oscilloscope	KEYSIGHT DSA91304A
Probes	1169B
Temperature	25°C
VDD / Vref-CA	1.200V / 0.600V

■ System picture



Summary & Conclusion

Judgment & Summary

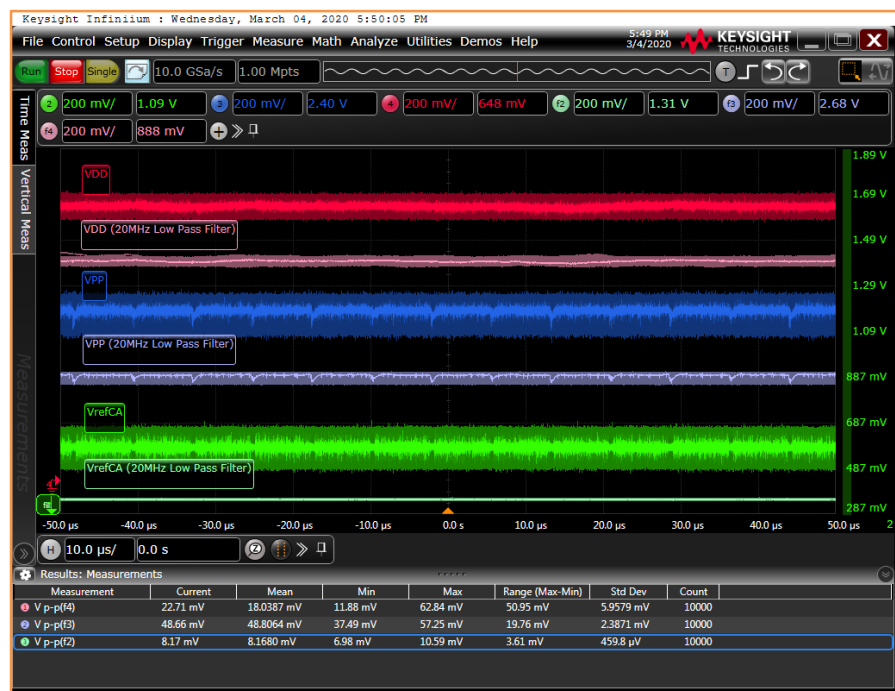
PASS

- The clock period time of this system is 0.758ns and operating frequency is about 1320Mhz. So, we applied with DDR4-2666 criteria value of JEDEC standard.
- This system doesn't have the power switch. So, we don't measure power-up sequence values.

Measurement Item	Result	Remark
Power Up Sequence Check	N/A	
Power Noise Check	Spec In.	- No problem.
Signal Integrity Check	Spec In.	- No problem.

Power Noise Check Result

■ VDD / VPP / Vref_CA - with DRAM stress test

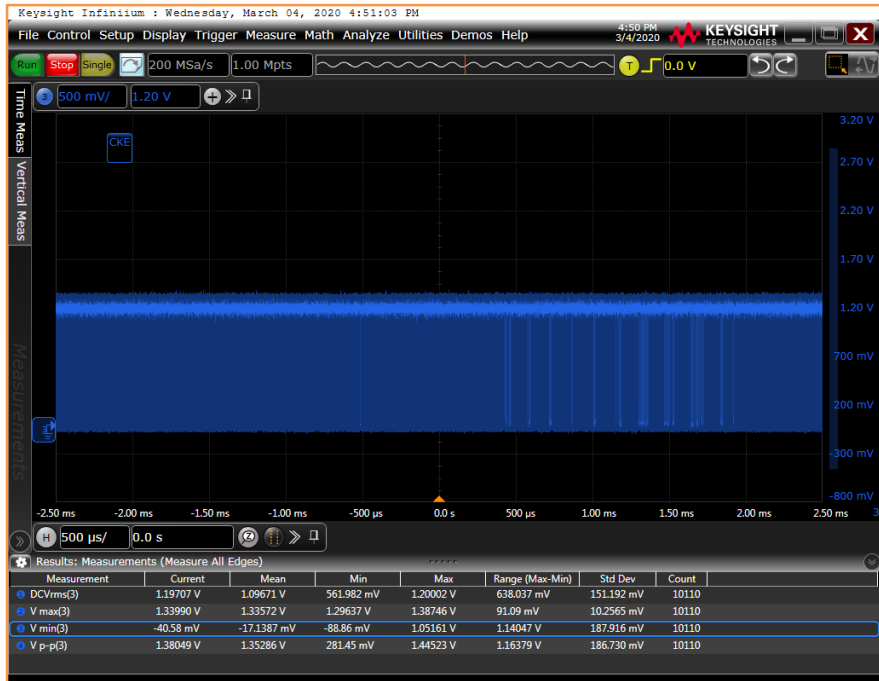


Parameter	Spec (AC+DC)	Peak to Peak	Remark
VDD	TBD	63mV	-
VPP	TBD	57mV	-
Vref-CA	≤ 24mV (VDD±1%)	11mV	Spec. in

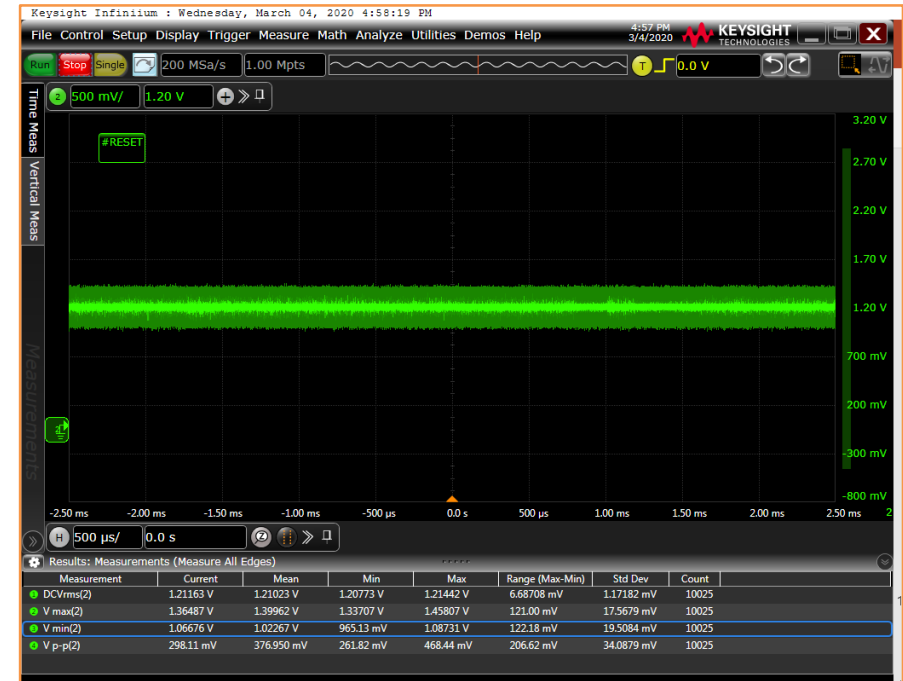
* SK hynix measured VDD/ VPP / Vref_CA including AC+DC (Low Pass Filter 20MHz) noise.

CKE & /RESET Signal Check Result

■ CKE Level in System Operation



■ /RESET Level in System Operation



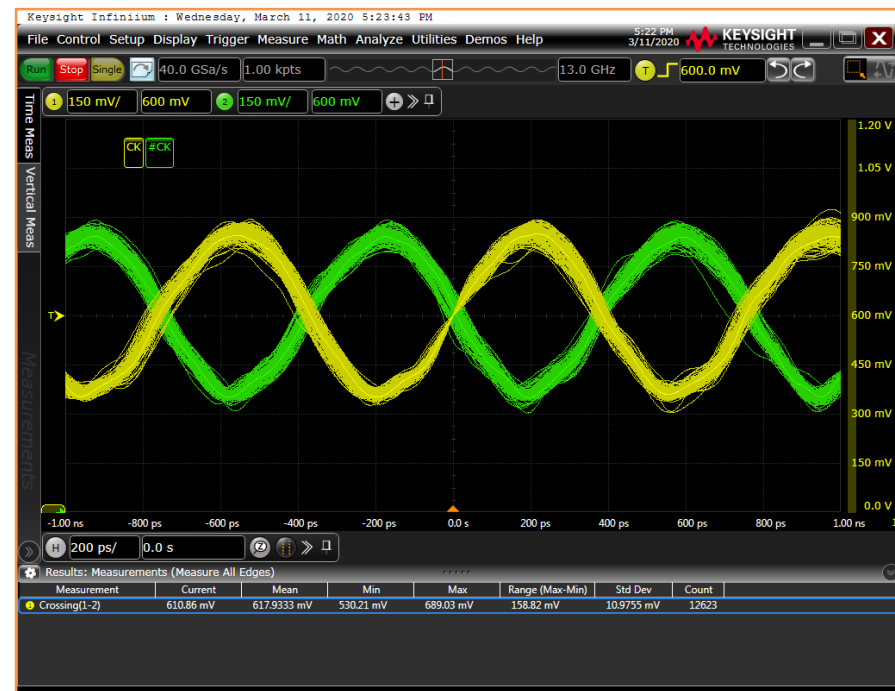
Parameter	Measurement	Remark
CKE Level	Vmin : -89mV	Power-down & Self-refresh mode used.
/RESET Level	Vmin : 965mV	High state stable

Signal Integrity Test Result (Clock)

■ Clock with differential



■ CLK VIX



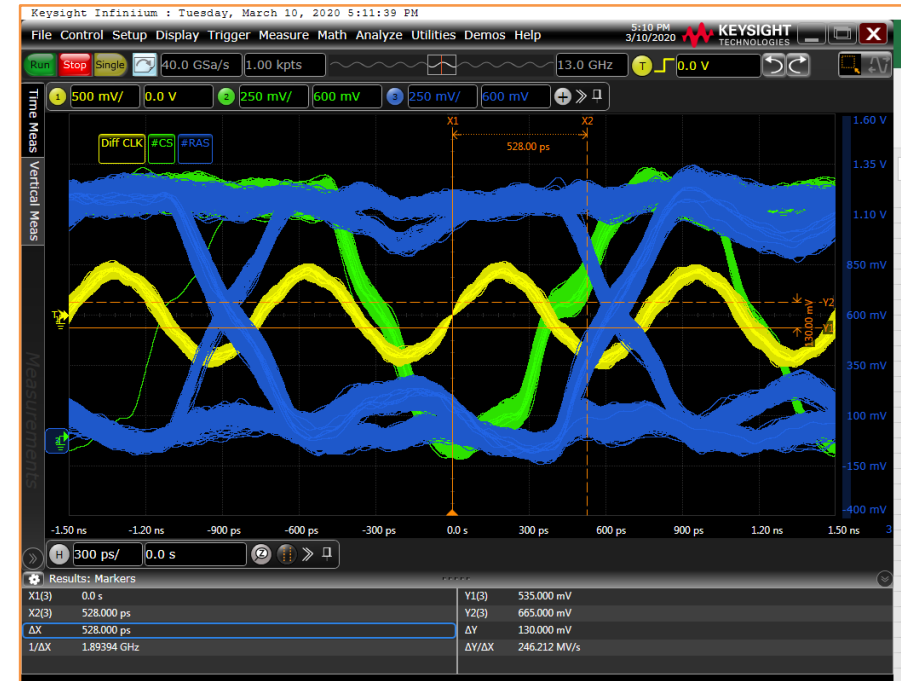
Parameter	Spec		Measurement	Remark
	Min	Max		
Clock Cycle Time (tCK)	0.750ns	0.833ns	0.758ns	Spec. in
Clock High Level Width (tCH)	364ps(0.48tCK)	394ps(0.52tCK)	376ps (0.496tCK)	Spec. in
Clock Low Level Width (tCL)	364ps(0.48tCK)	394ps(0.52tCK)	382ps (0.504tCK)	Spec. in
Clock Period Jitter (JIT_per)	-38ps	38ps	-30 / 36	Spec. in
VIH diff(ac)	0.180V	-	0.470V	Spec. in
VIL diff(ac)	-	-0.180V	-0.472V	Spec. in
Clock VIX	0.480V	0.720V ₈	0.530V / 0.689V	Spec. in

Signal Integrity Test Result (Command / Address)

■ CS#_U505



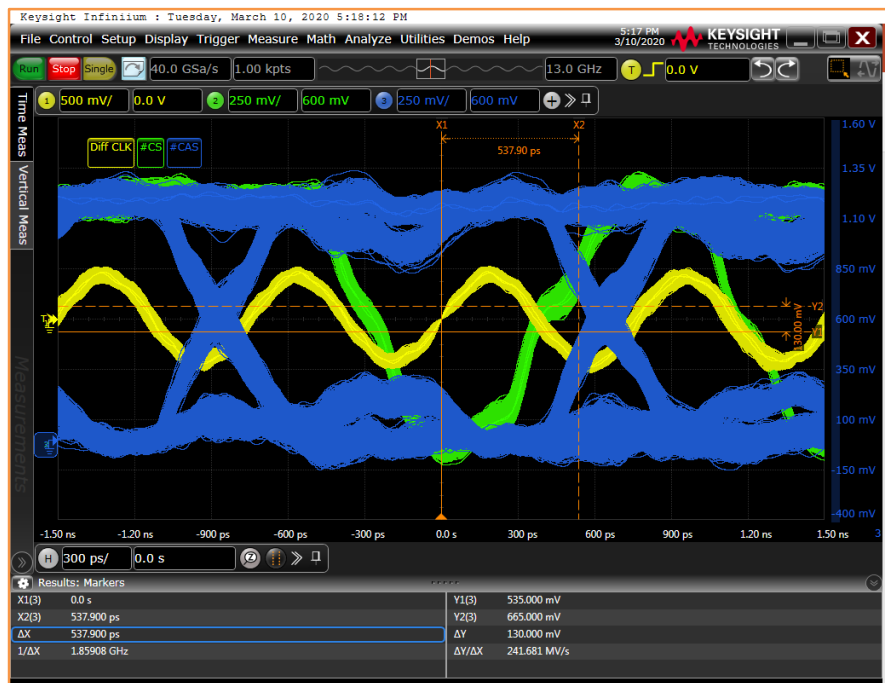
■ RAS#_U505



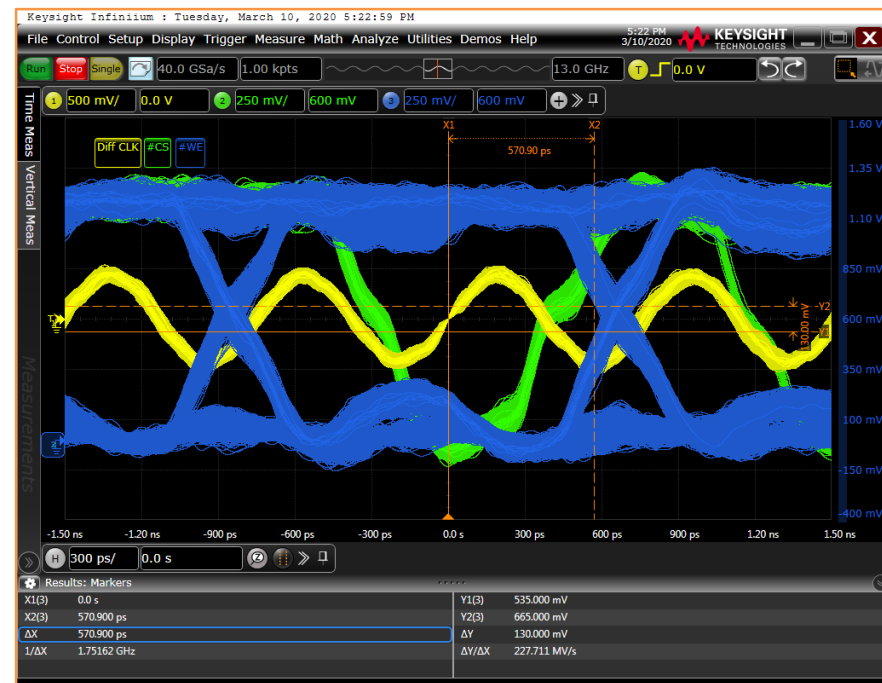
Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	CS#	RAS#	
tIS(Base)	55 ps	-	198ps	746ps	Spec. in
tIH(Base)	80 ps	-	330ps	528ps	Spec. in

Signal Integrity Test Result (Command / Address)

■ CAS#_U505



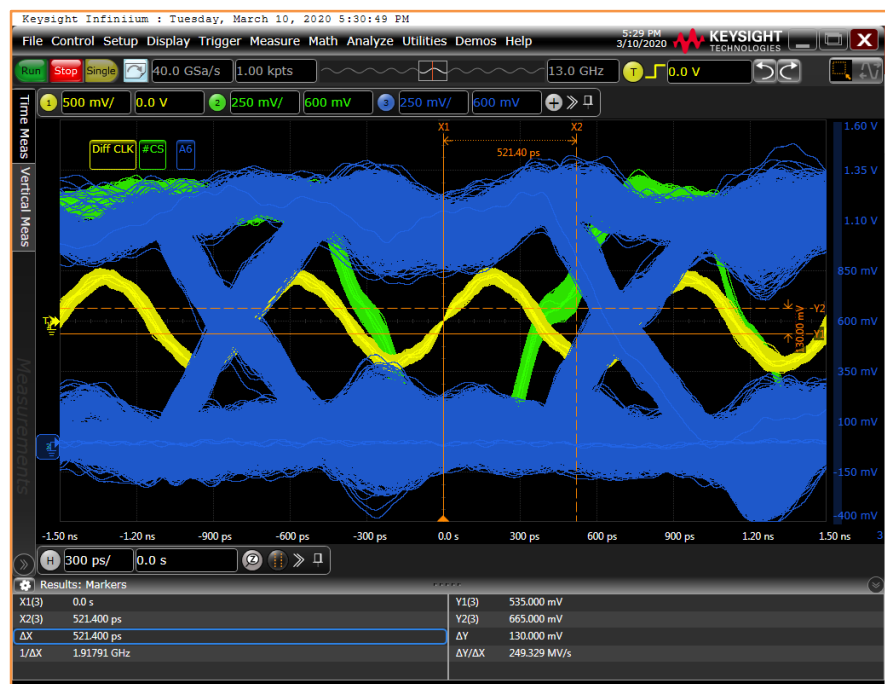
■ WE#_U505



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	CAS#	WE#	
tIS(Base)	55 ps	-	752ps	733ps	Spec. in
tIH(Base)	80 ps	-	538ps	571ps	Spec. in

Signal Integrity Test Result (Command / Address)

■ ADD6_U505



Parameter	Spec.		Measurement	Remark
Unit : ps	Min	Max	ADD6	
tIS(Base)	55 ps	-	650ps	Spec. in
tIH(Base)	80 ps	-	521ps	Spec. in

Signal Integrity Test Result (Data strobe / Data)

■ VIHL_AC_U505_DQL



■ VIHL_AC_U505_DQU



Parameter	Spec.		Measurement		Remark
Unit : mV	Min	Max	DQL	DQU	
VIHL	150 mV	-	532mV	542mV	Spec. in

Signal Integrity Test Result (Data strobe / Data)

■ TdIPW_U505_DQL



■ TdIPW_U505_DQU



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	DQL	DQU	
TdIPW	211 ps (0.58 UI)	-	286ps	264ps	Spec. in

Signal Integrity Test Result (Data strobe / Data)

■ TdIVW_total / VdIVW_total_U505_DQL ※  : Spec. Zone

■ TdIVW_total / VdIVW_total_U505_DQU



Parameter	Spec.		Measurement		Remark
Unit : ps, mV	Min	Max	DQL	DQU	
TdIVW_total	-	80 ps (0.22 UI)	Spec. In	Spec. In	1 UI = 364 ps
VdIVW_total	-	120 mV	Spec. In	Spec. In	Vcent_DQ = $\Delta V_{IHL}/2$

Signal Integrity Test Result (Data strobe / Data)

■ tDQSS_U505_DQSL



■ tDQSS_U505_DQSU



Parameter	Spec.		Measurement		Remark
Unit : ps	Min	Max	DQSL	DQSU	
tDQSS	-205 (-0.27tCK)	205 (+0.27tCK)	43ps	86ps	Spec. in

Thank you

